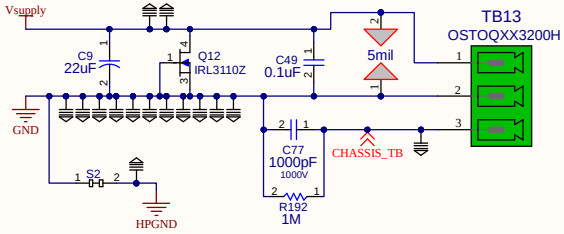
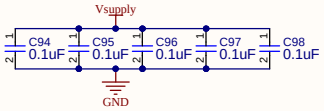
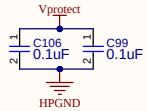
POWER INPUT (10-28V)

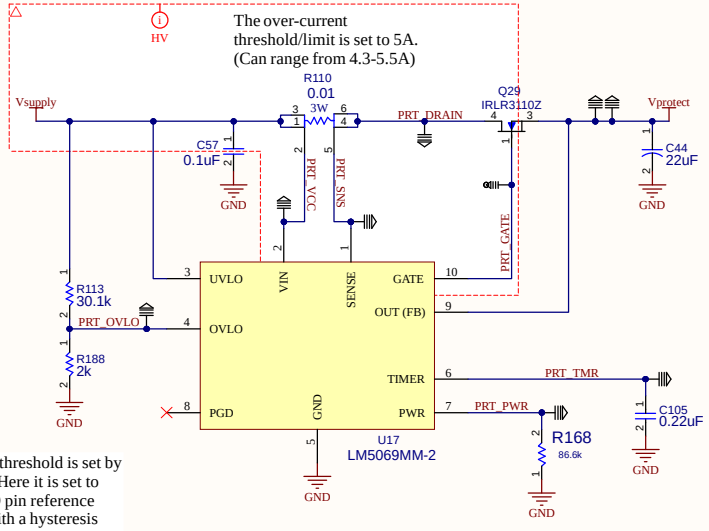


(Vsupply bypassing at the back row terminal blocks and the motor connectors)



(Vprotect bypassing at the front row terminal blocks)





The over-voltage threshold is set by R113 and R188. Here it is set to 40V. (The OVLO pin reference voltage is 2.5V with a hysteresis current of 21uA.)

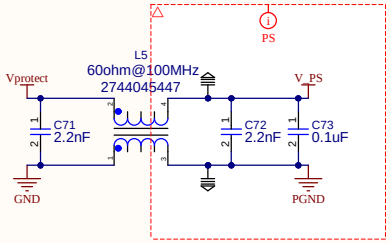
* OV events turn off the output immediately. (There is no timer like there is for OC or OP events.)

C105 sets the OC/OP timeout for U17. With 0.22uF, the following timing sequence is followed:

* An OC or OP event will be regulated to the set limits (5A or 25W in the FET) for 10ms. If the event hasn't ended by then, the output is shut off.

* The chip has a 0.5% fault duty cycle, so the cooldown time is 2s. (Calculated from 10ms/0.005) After this time the output is turned back on.

* The cycle repeats as long as the problem is present.



V_PS only powers the buck converters on the Power_Supply page.

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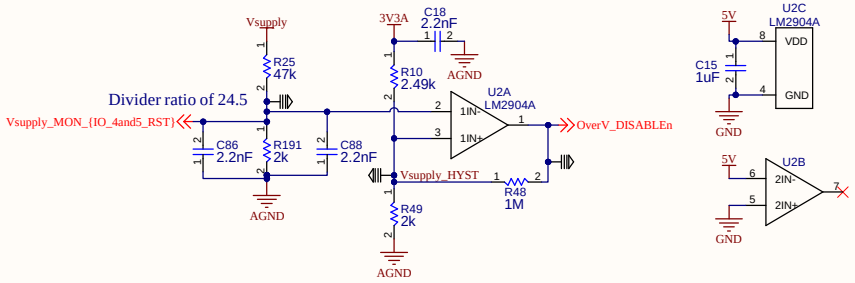
Sheet Name: Power_Input.SchDoc		
Assembly Number: 1108700	Revision: K1	
Date: 12/15/2023 Time: 9:52:21 AM	Sheet 1 of 14	Author: DP

POWER SUPPLIES

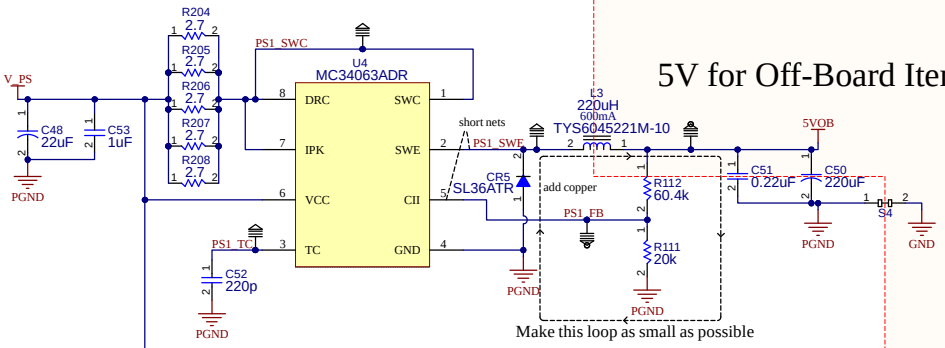
OVERV TRIP

This is set to trip at about 36.2V and will reset with a hysteresis of 0.4V. "OverV_DISABLEn" only disables the motor driver IC, and isn't read by the MCU. However, the MCU can also disable the motor driver IC by briefly setting "Vsupply-MON_{IO_4and5_RST}" as an output and pulling it high.

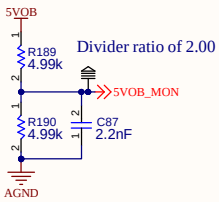


5V for Off-Board Items

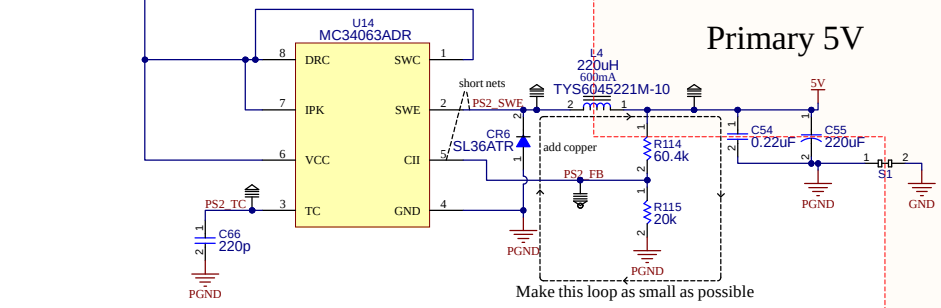
5VOB output current is limited to about 500mA with a 10V input. As input voltage increases the current limit increases slightly to about 550mA at 24V.



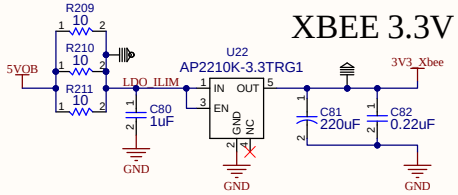
5V set-point for both converters is 5.01V +-3%.



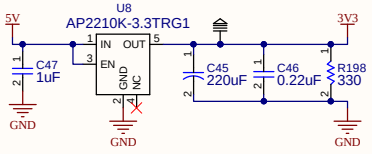
Primary 5V



XBEE 3.3V

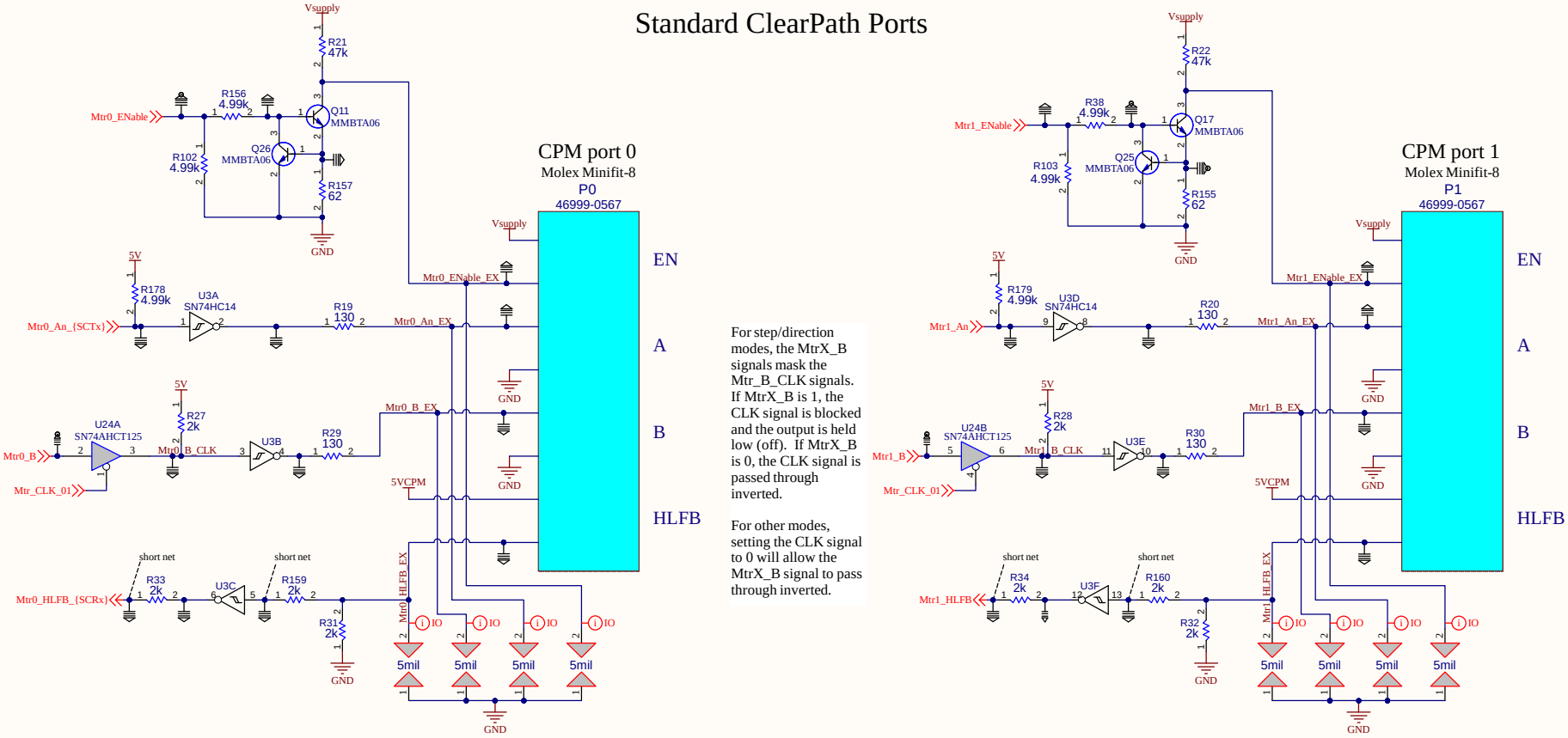


MCU 3.3V



Project Title:	***ClearCore Electrical Schematic***		
Sheet Name:	Power_Supply.SchDoc		*Teknic, Inc.* *115 Victor Heights Parkway* *Victor, NY 14564* *(585) 784-7454*
Assembly Number:	1108700	Revision: K1	
Date: 12/15/2023	Time: 9:52:21 AM	Sheet 2 of 14	Author: DP

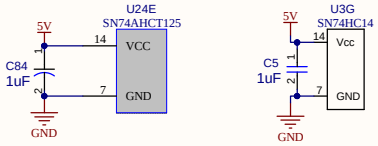
Standard ClearPath Ports

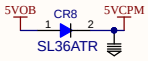


For step/direction modes, the MtrX_B signals mask the Mtr_B_CLK signals. If MtrX_B is 1, the CLK signal is blocked and the output is held low (off). If MtrX_B is 0, the CLK signal is passed through inverted.

For other modes, setting the CLK signal to 0 will allow the MtrX_B signal to pass through inverted.

Port CP0 can also be used as a serial port. The intention is to use this to connect to a ClearIO specific SC Hub. As the net names suggest, Mtr0_An_{SCTx} above is TX and Mtr0_HLFB_{SCRx} is RX for SERCOM 3. The other two outputs (Mtr0_ENable and Mtr0_B) serve no serial port purpose but could be used for other SC Hub functions.

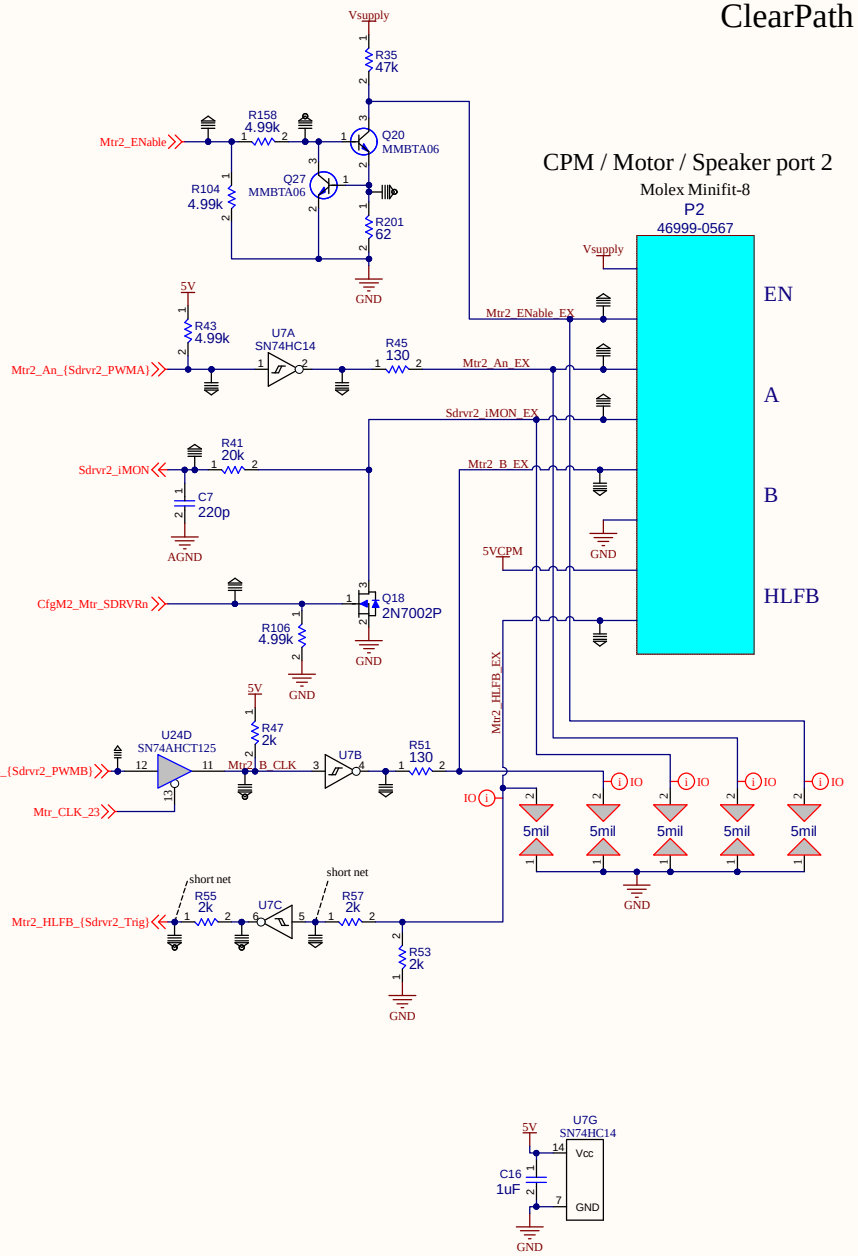


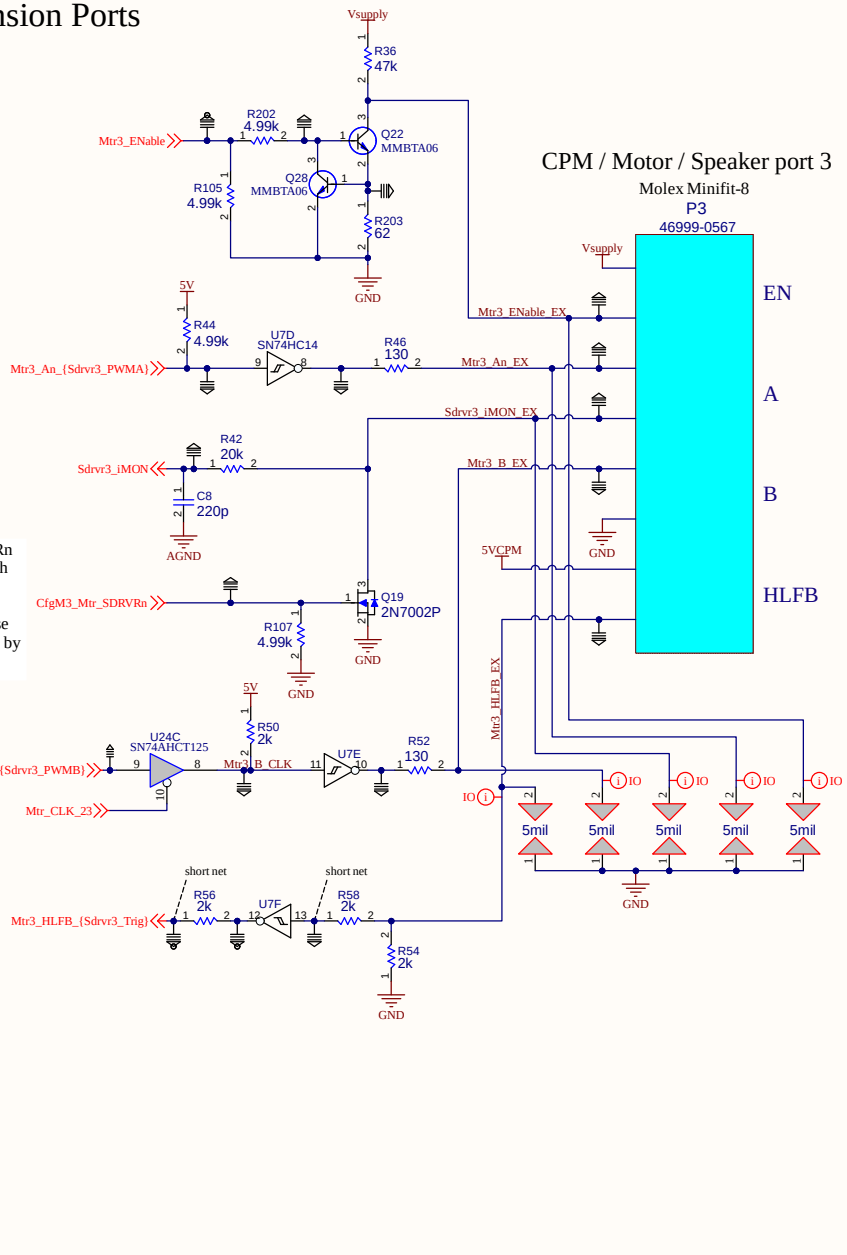


This diode protects the 5VOB supply in case 24V is accidentally connected to the 5V pins on the CPM connectors.

Project Title:	***ClearCore Electrical Schematic***		
Sheet Name:	Basic_CPM_Control.SchDoc		*Teknic, Inc.* *115 Victor Heights Parkway* *Victor, NY 14564* *(585) 784-7454*
Assembly Number:	1108700	Revision: K1	
Date: 12/15/2023	Time: 9:52:21 AM	Sheet 3 of 14	Author: DP

ClearPath / Motor-Expansion Ports

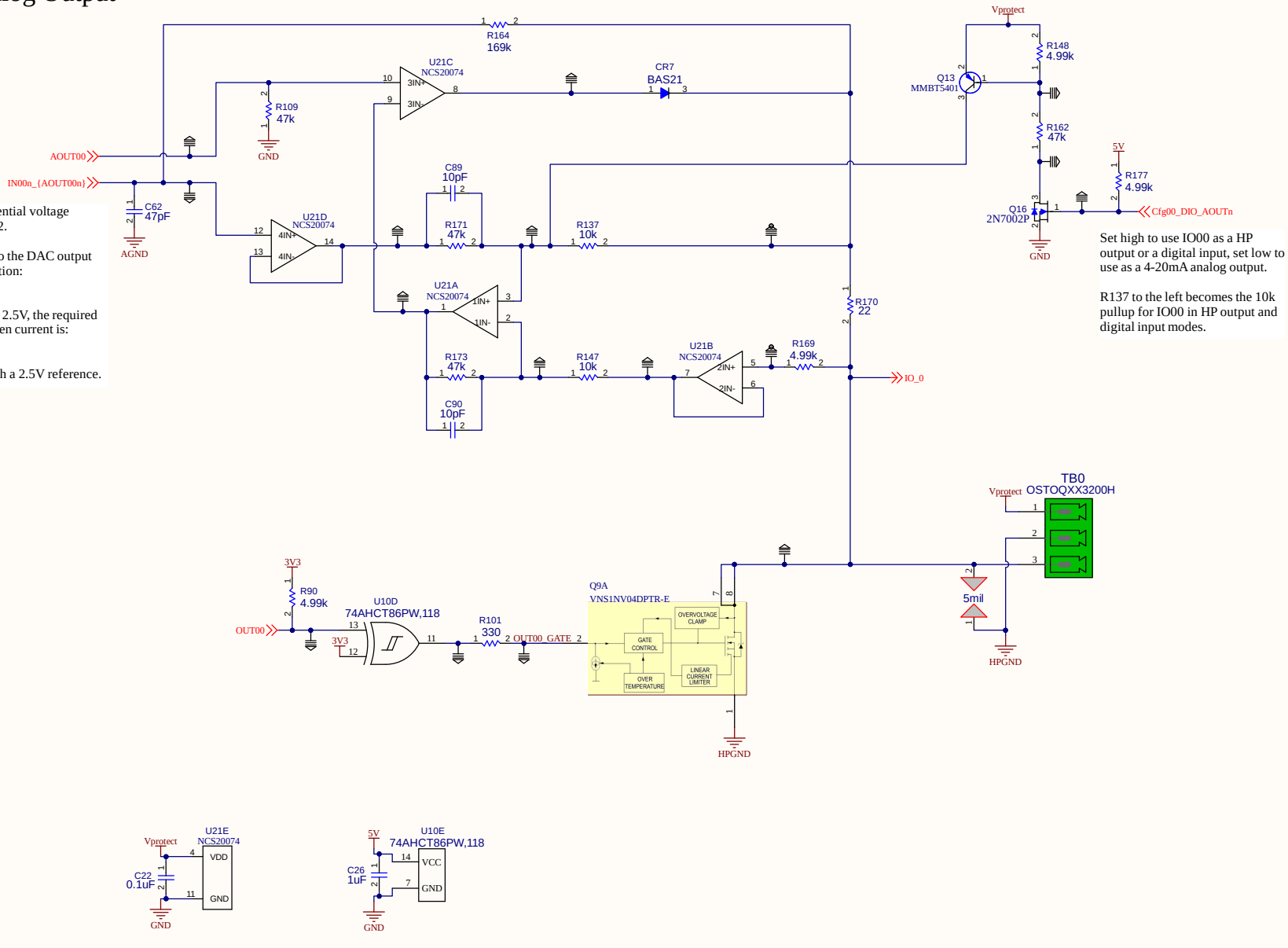




Set CfgMX_Mtr_SDRVRn high to use with ClearPath (output to a Ch A input). Set low to use with a screwdriver (current-sense return). These are driven by the shift register chain.

Project Title: *ClearCore Electrical Schematic*		*Teknic, Inc.*
Sheet Name: Combo_CPM_Screwdriver_Control.SchDoc		*115 Victor Heights Parkway*
Assembly Number: 1108700	Revision: K1	*Victor, NY 14564*
Date: 12/15/2023 Time: 9:52:21 AM	Sheet 4 of 14	*(585) 784-7454*
		Author: DP

4-20mA Analog Output



As of rev F, DACV is a differential voltage centered around DAC VREF/2.

The output current is related to the DAC output voltage by the following equation:
mA = DACV * 9.671

Therefore, with a reference of 2.5V, the required 11-bit value required for a given current is:
DATA0 = mA * 84.664

Full range is 0.0 - 24.1mA with a 2.5V reference.

Set high to use IO00 as a HP output or a digital input, set low to use as a 4-20mA analog output.

R137 to the left becomes the 10k pullup for IO00 in HP output and digital input modes.

Project Title: *ClearCore Electrical Schematic*		Teknic, Inc. 115 Victor Heights Parkway Victor, NY 14564 (585) 784-7454
Sheet Name: Analog_Out.SchDoc		
Assembly Number: 1108700	Revision: K1	
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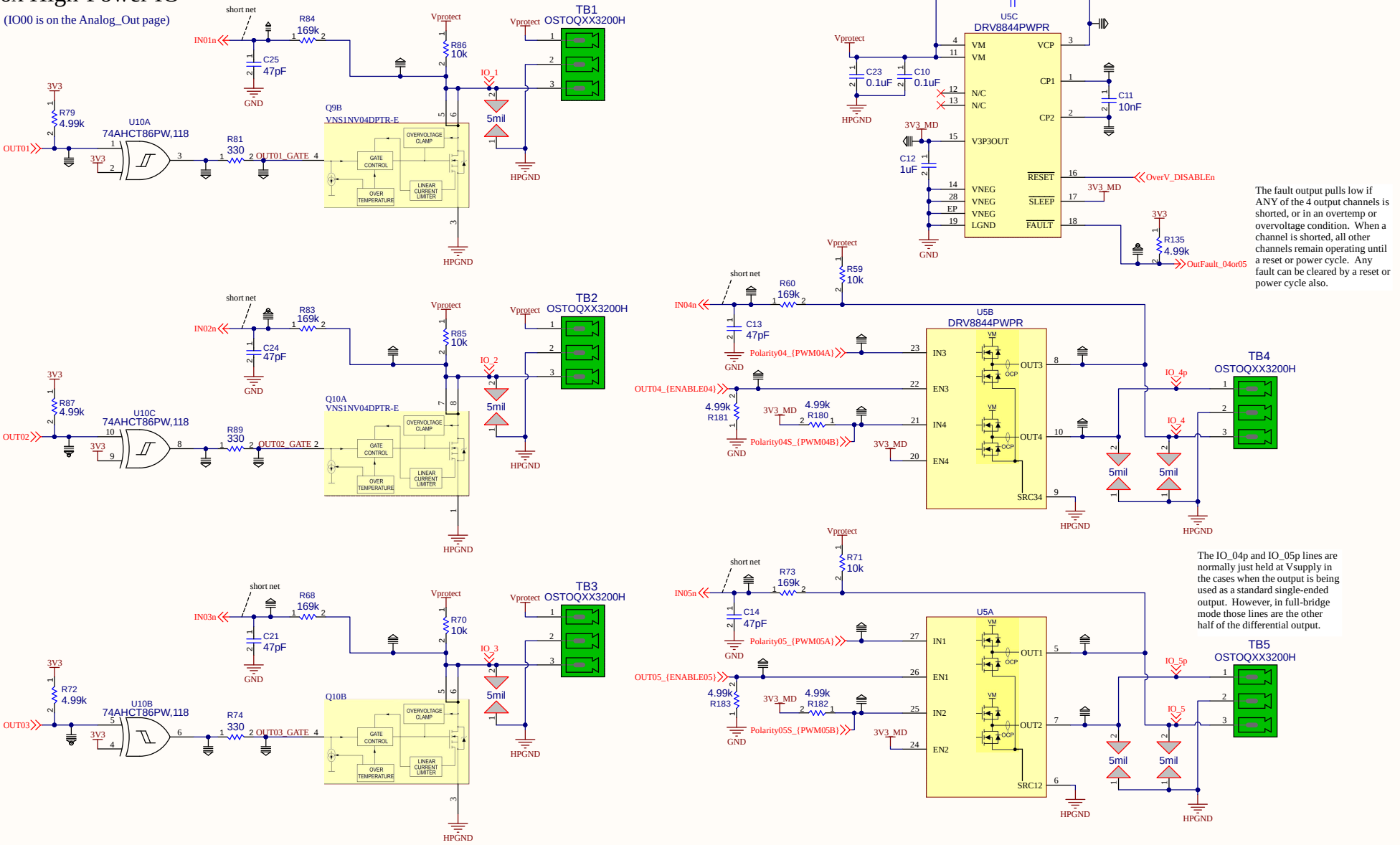
6x High-Power IO

(IO00 is on the Analog_Out page)

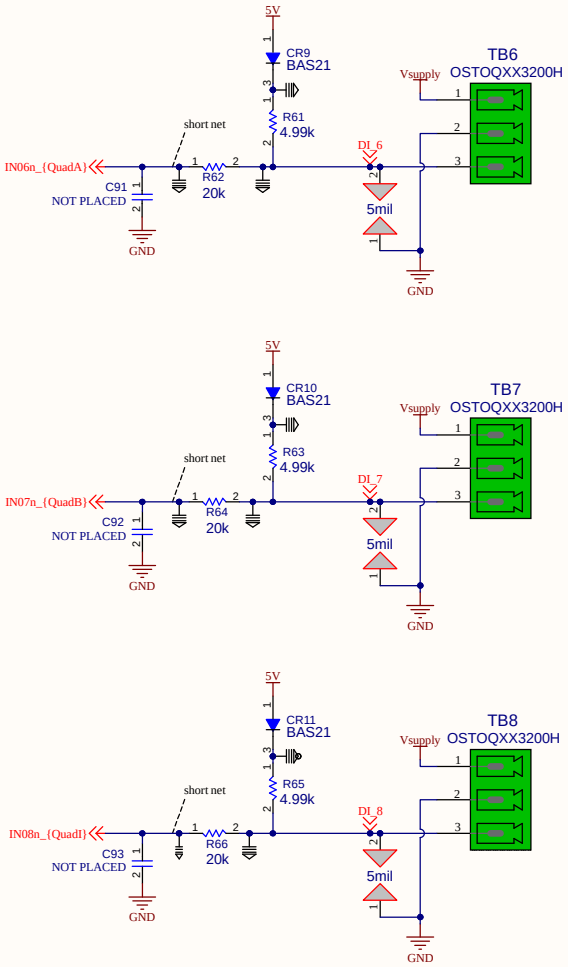


The fault output pulls low if ANY of the 4 output channels is shorted, or in an overtemp or overvoltage condition. When a channel is shorted, all other channels remain operating until a reset or power cycle. Any fault can be cleared by a reset or power cycle also.

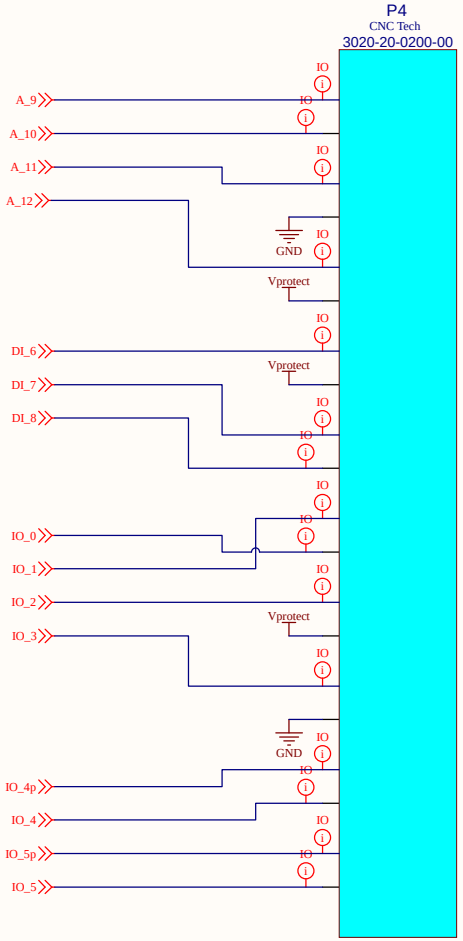
The IO_04p and IO_05p lines are normally just held at Vsupply in the cases when the output is being used as a standard single-ended output. However, in full-bridge mode those lines are the other half of the differential output.

Project Title:	*ClearCore Electrical Schematic*		
Sheet Name:	High_Power_Out_In.SchDoc		Teknic, Inc. 115 Victor Heights Parkway Victor, NY 14564 (585) 784-7454
Assembly Number:	1108700	Revision: K1	
Date: 12/15/2023	Time: 9:52:21 AM	Sheet 6 of 14	Author: DP

3x Digital/QDEC IN

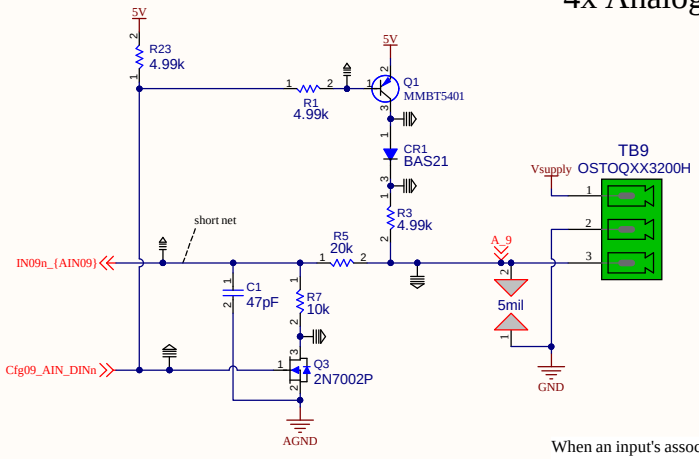


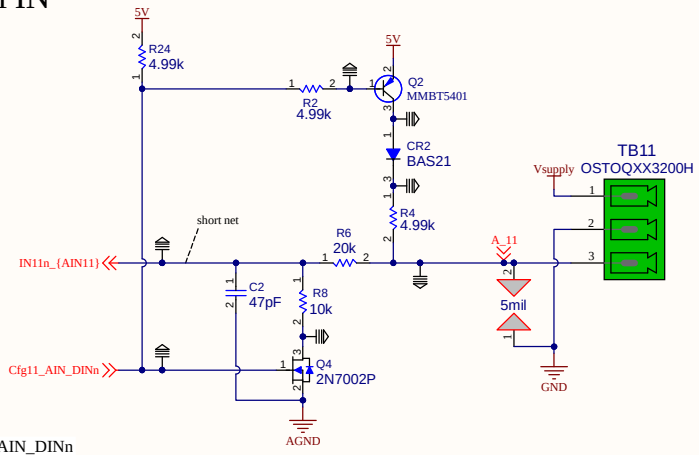
Combined IO Header



Project Title:	***ClearCore Electrical Schematic***		*Teknic, Inc.*
Sheet Name:	Digital_In_and_Combined_Header.SchDoc		*115 Victor Heights Parkway*
Assembly Number:	1108700	Revision: K1	*Victor, NY 14564*
Date: 12/15/2023	Time: 9:52:21 AM	Sheet 7 of 14	*(585) 784-7454*
			Author: DP

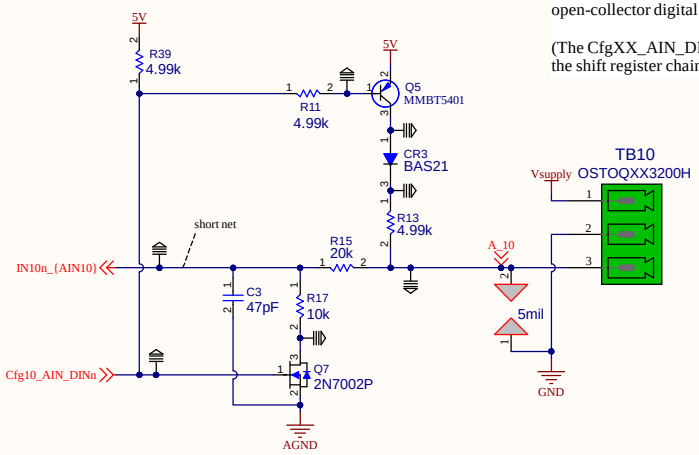
4x Analog/Digital IN

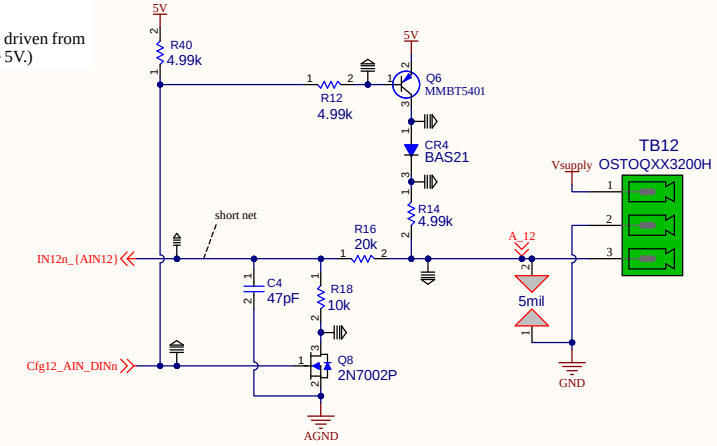




When an input's associated CfgXX_AIN_DINn line is set high, the lower FET turns on, enabling a voltage divider that allows 0-10V analog in. When the line is set low, the upper BJT is on, enabling a 5V pull-up to allow open-collector digital inputs.

(The CfgXX_AIN_DINn lines are driven from the shift register chain, so they are 5V.)



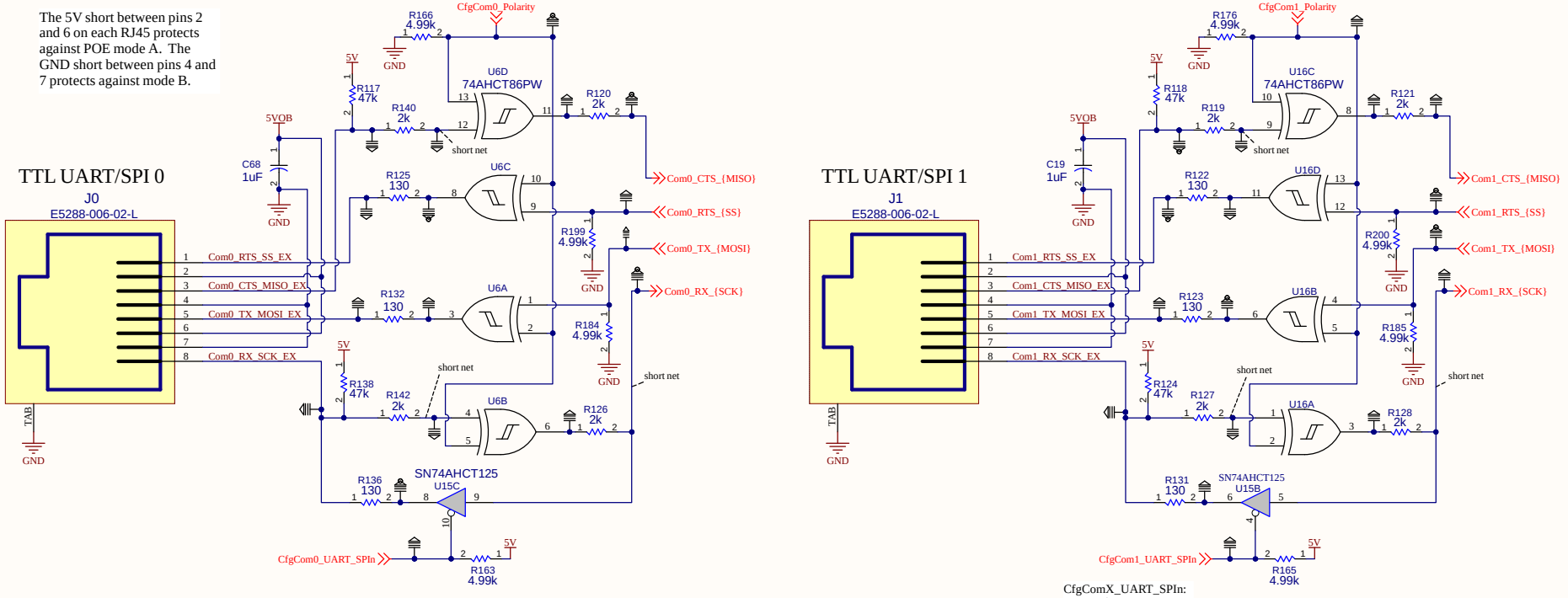


Project Title: *ClearCore Electrical Schematic*		
Sheet Name: Analog_Digital_In.SchDoc		*Teknic, Inc.* *115 Victor Heights Parkway* *Victor, NY 14564* *(585) 784-7454*
Assembly Number: 1108700	Revision: K1	
Date: 12/15/2023 Time: 9:52:22 AM	Sheet 8 of 14	Author: DP

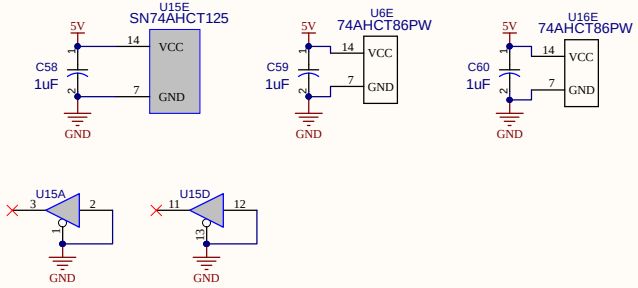
Off-Board Serial Interfaces

The 5V short between pins 2 and 6 on each RJ45 protects against POE mode A. The GND short between pins 4 and 7 protects against mode B.

CfgComX_Polarity:
In UART mode set low for non-inverted TTL or set high for inverted "RS232".
(Just leave low in SPI mode.)

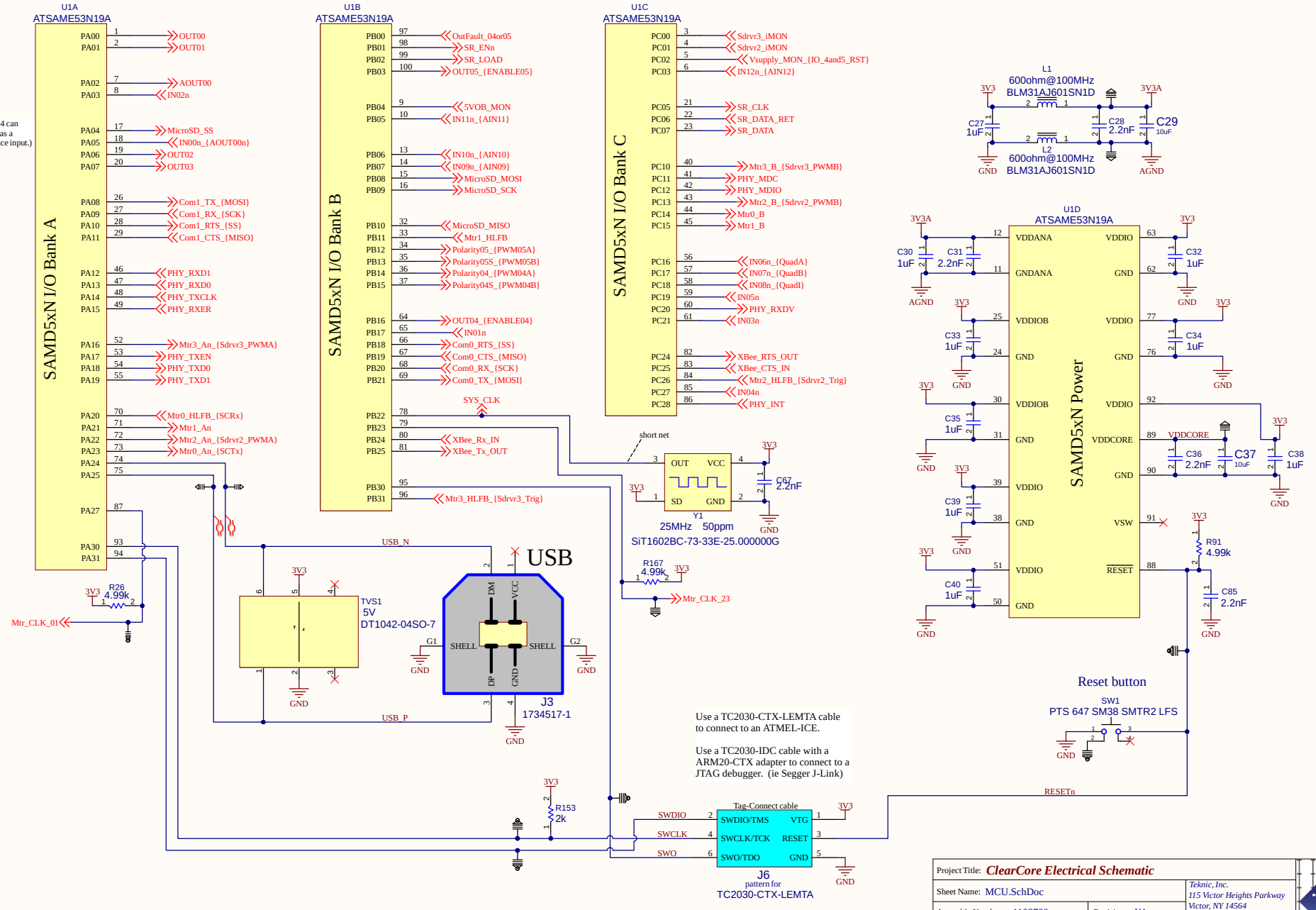


CfgComX_UART_SPIn:
Set low for SCK (SPI) or set high for RX (UART).



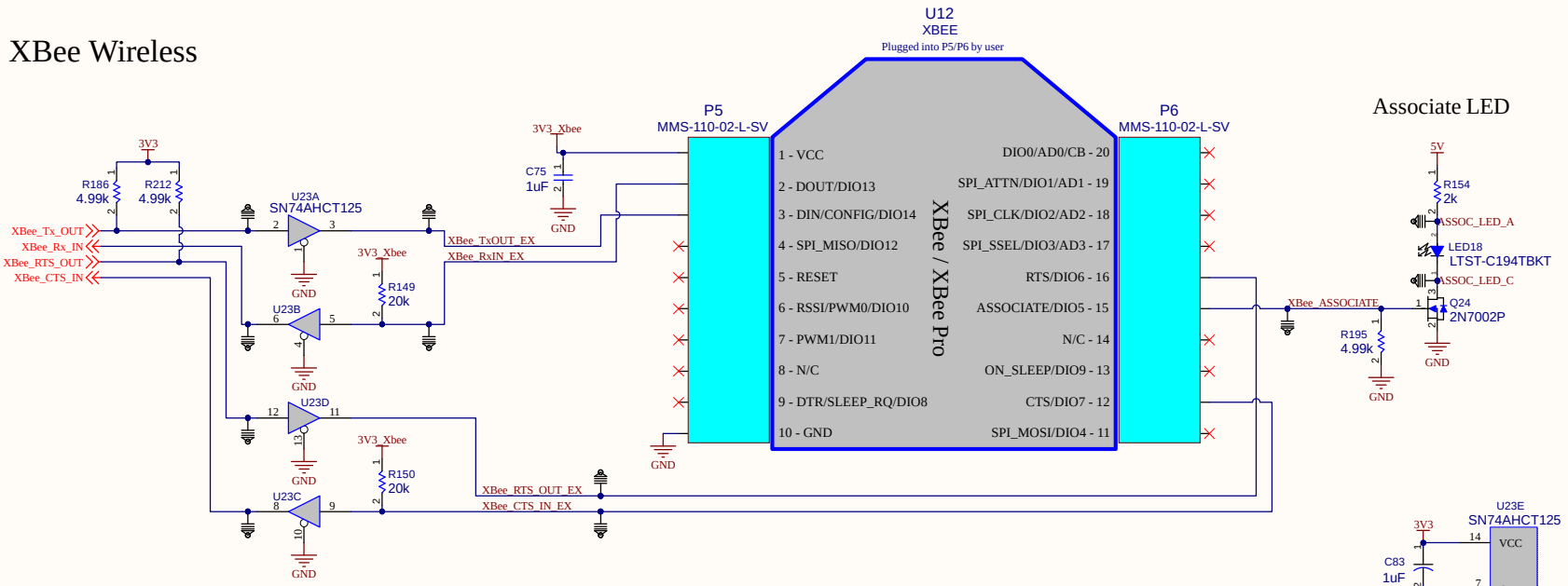
Project Title:	***ClearCore Electrical Schematic***		*Teknic, Inc.*
Sheet Name:	Serial_Interfaces.SchDoc		*115 Victor Heights Parkway*
Assembly Number:	1108700	Revision: K1	*Victor, NY 14564*
Date: 12/15/2023	Time: 9:52:22 AM	Sheet 9 of 14	*(585) 784-7454*
			Author: DP

Processor

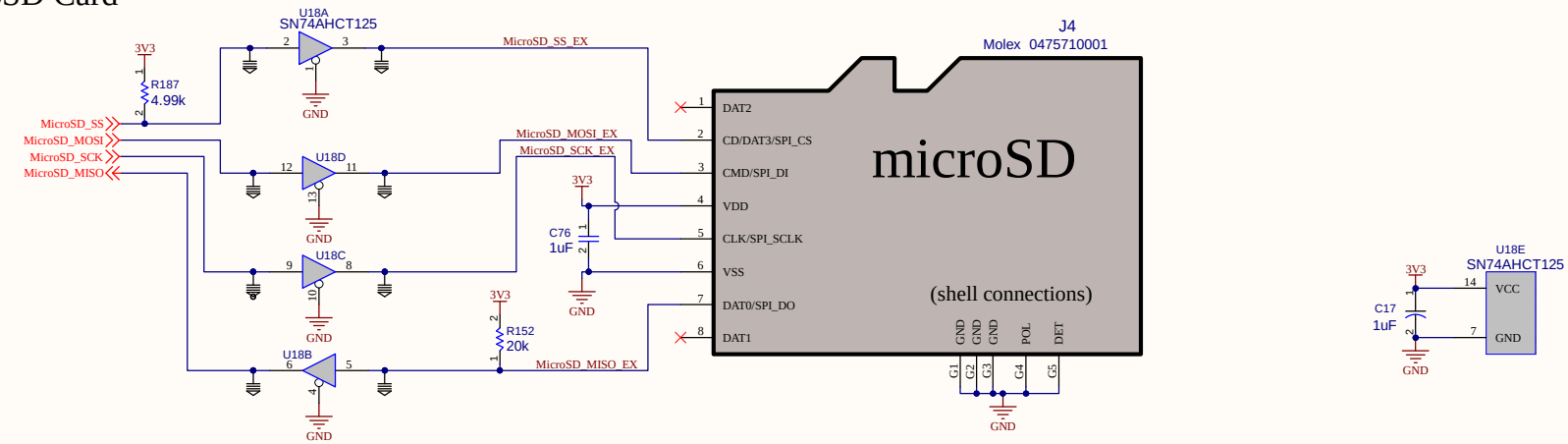


Project Title:	*ClearCore Electrical Schematic*		*Teknic, Inc.*
Sheet Name:	MCU.SchDoc		*115 Victor Heights Parkway*
Assembly Number:	1108700	Revision: K1	*Victor, NY 14564*
Date: 12/15/2023	Time: 9:52:22 AM	Sheet 10 of 14	*(585) 784-7454*
		Author: DP	

XBee Wireless

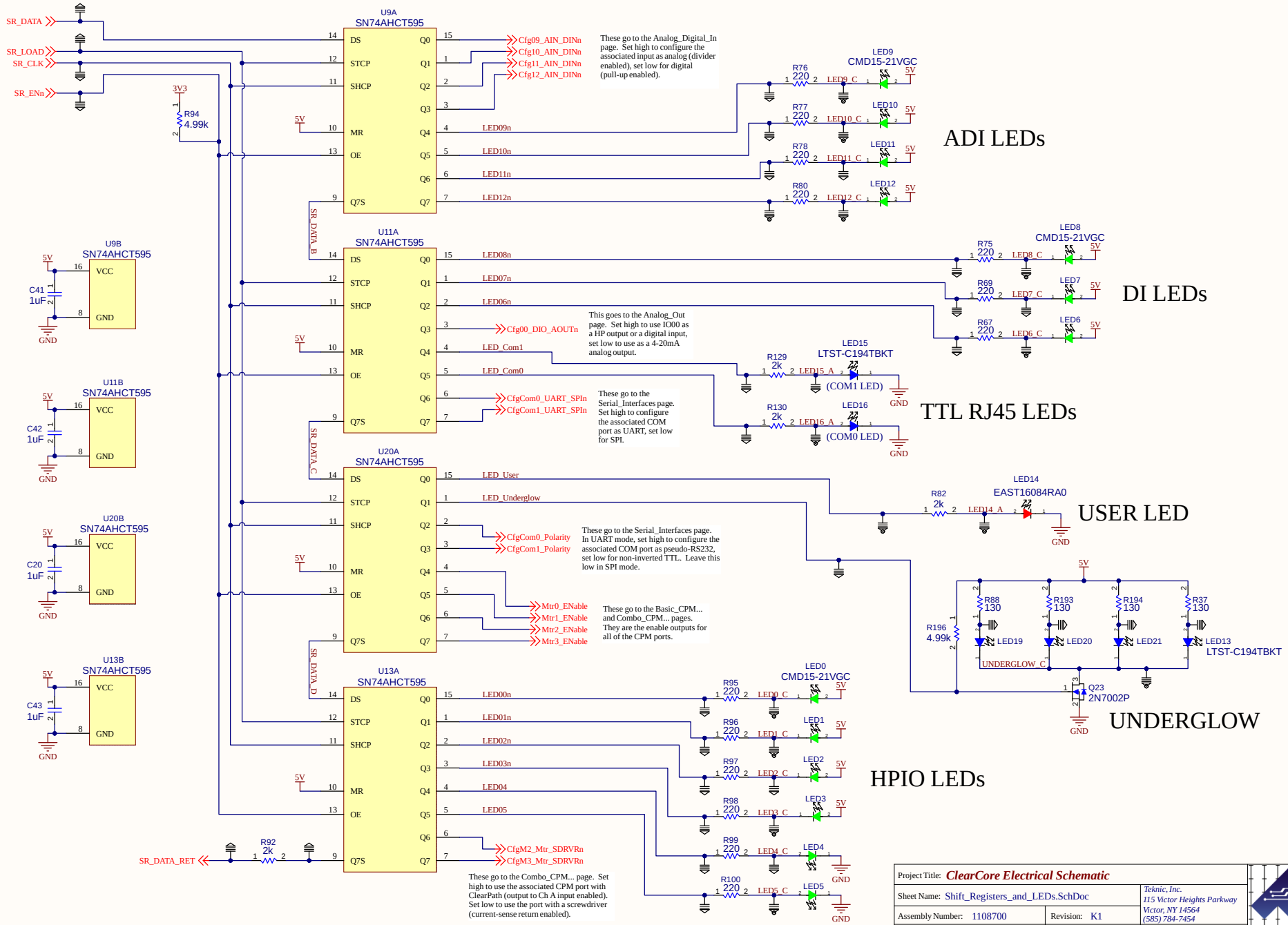


microSD Card



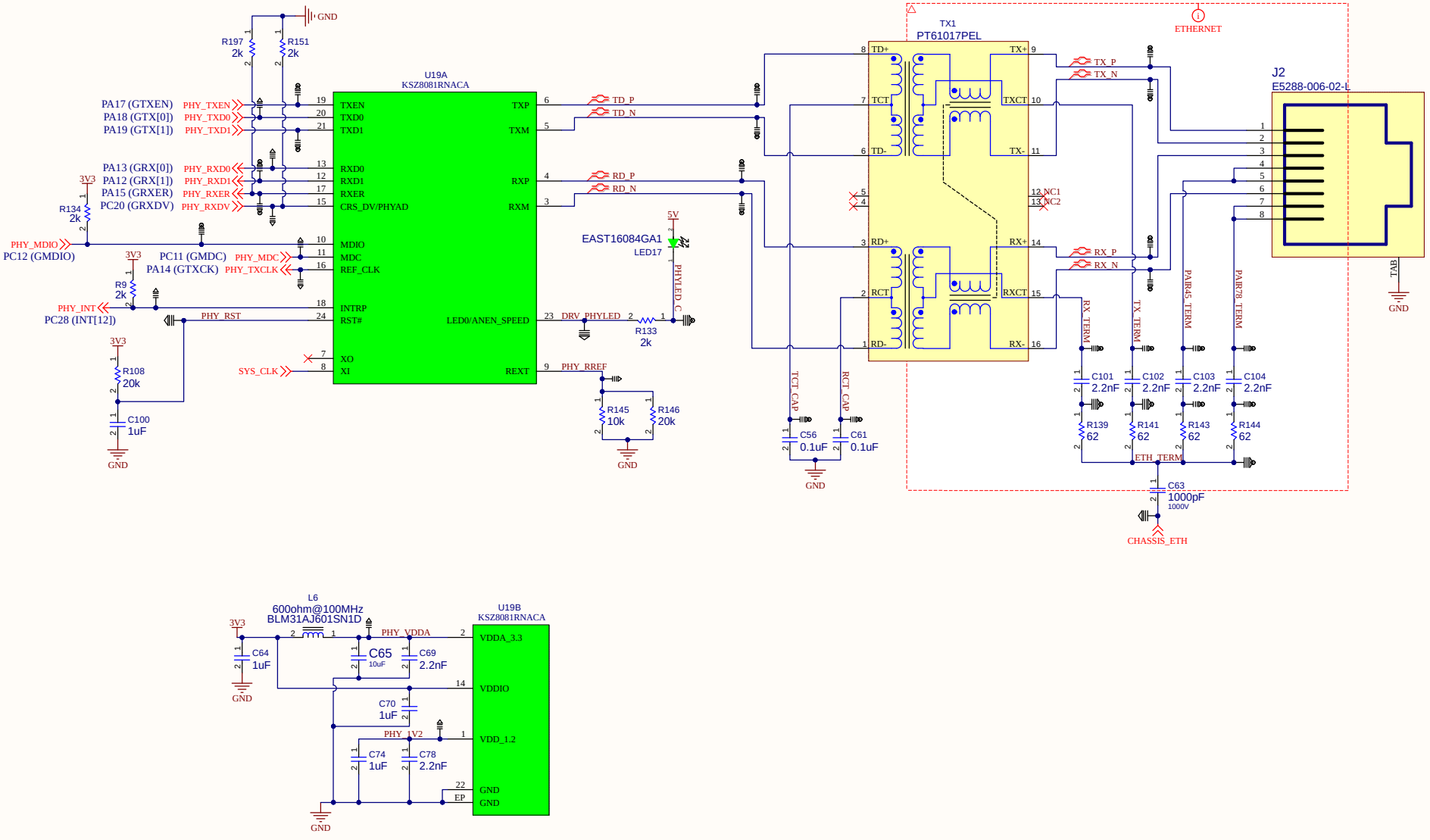
Project Title:	***ClearCore Electrical Schematic***		*Teknic, Inc.*
Sheet Name:	Xbee_and_microSD.SchDoc		*115 Victor Heights Parkway*
Assembly Number:	1108700	Revision: K1	*Victor, NY 14564*
Date: 12/15/2023	Time: 9:52:22 AM	Sheet 11 of 14	*(585) 784-7454*
			Author: DP

SPI Shift Register Chain for LEDs and hardware configuration



Project Title:	***ClearCore Electrical Schematic***		*Teknic, Inc.*
Sheet Name:	Shift_Registers_and_LEDs.SchDoc		*115 Victor Heights Parkway*
Assembly Number:	1108700	Revision: K1	*Victor, NY 14564*
Date: 12/15/2023	Time: 9:52:22 AM	Sheet 12 of 14	*(585) 784-7454*
			Author: DP

Ethernet



Project Title:	***ClearCore Electrical Schematic***		
Sheet Name:	Ethernet.SchDoc		*Teknic, Inc.* *115 Victor Heights Parkway* *Victor, NY 14564* *(585) 784-7454*
Assembly Number:	1108700	Revision: K1	
Date: 12/15/2023	Time: 9:52:22 AM	Sheet 13 of 14	Author: DP

Mounting Holes Etc

Spare testpoints

Fiducials

FID1 FID4

FID2 FID5

FID3 FID6

PWB

BOARD

1108701_K

Mounting Points

CHASSIS

MT1
Assembly mount point

MT2
Assembly mount point

KEYHOLE
PEM
PEM1

KEYHOLE
PEM
PEM2

KEYHOLE
PEM
PEM3

CHASSIS_ETH

MT3
Board-plate mount point

(Center, near the USB connector)

CHASSIS_TB

MT4
Mounting hole

(Bottom right, near the PWR connector)

Project Title: *ClearCore Electrical Schematic*		*Teknic, Inc.* *115 Victor Heights Parkway* *Victor, NY 14564* *(585) 784-7454*
Sheet Name: MountingHolesEtc.SchDoc		
Assembly Number: 1108700	Revision: K1	
Date: 12/15/2023 Time: 9:52:22 AM	Sheet 14 of 14	Author: DP